Description

SPARK CURRENT CANCELLATION IN CHARGE PUMP OF HIGH SPEED PHASE LOCK LOOP CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Technical Field

[0002] The present invention relates to a structure and associated method to remove extra current from a phase lock loop circuit.

[0003] 2. Related Art

[0004] An electrical circuit typically comprises unwanted signals. Unwanted signals may cause the electrical circuit to malfunction. Therefore there exists a need to remove unwanted signals from an electrical circuit.

SUMMARY OF INVENTION

[0005] The present invention provides a phase lock loop circuit, comprising:

[0006] a voltage controlled oscillator adapted to provide a first

signal comprising a first frequency;

[0007] a phase comparator adapted to compare the first signal comprising the first frequency to a reference signal comprising a reference frequency, wherein the phase comparator is further adapted to provide a control signal representing a phase difference between the first signal and the reference signal; and

[0008] a charge pump circuit adapted to receive the control signal and control the voltage controlled oscillator such that a phase of the first signal equals a phase of the reference signal, wherein the charge pump circuit is further adapted to compensate for a spark current resulting from a switching mode of the control signal.

[0009] The present invention provides a method, comprising:

[0010] providing by a voltage controlled oscillator, a first signal comprising a first frequency;

[0011] comparing by a phase comparator, the first signal comprising the first frequency to a reference signal comprising a reference frequency;

[0012] providing by the phase comparator, a control signal representing a phase difference between the first signal and the reference signal;

[0013] receiving by a charge pump circuit, the control signal;

[0014] controlling by the charge pump circuit, the voltage controlled oscillator such that a phase of the first signal is about equal to a phase of the reference signal; and

[0015] compensating by the charge pump circuit, for a spark current resulting from a switching mode of the control signal.

[0016] The present invention advantageously provides a structure and associated method to remove unwanted signals from an electrical circuit.

BRIEF DESCRIPTION OF DRAWINGS

[0017] FIG. 1 illustrates a schematic of a differential phase lock loop (PLL) circuit, in accordance with embodiments of the present invention.

[0018] FIG. 2 illustrates the schematic of the sub-circuit within the differential phase lock loop circuit of FIG. 1, in accordance with embodiments of the present invention.

[0019] FIG. 3 illustrates a modified schematic for the sub-circuit of FIG. 2, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0020] FIG. 1 illustrates a schematic of a differential phase lock loop (PLL) circuit 1 comprising a voltage controlled oscil-

lator (VCO) circuit 4, a phase comparator circuit 6, and a charge pump circuit 15, in accordance with embodiments of the present invention. The charge pump circuit 15 comprises a sub–circuit 10 (described in greater detail in the description of FIG. 2) for accepting a positive pulse increase (INC) signal (i.e., a control signal) and a sub–circuit 11 that is equivalent and symmetrical to the sub–circuit 10 for accepting a positive pulse decrease (DEC) signal (i.e., a control signal). A capacitor C_1 and a capacitor C_2 each comprise a same capacitance value C. A current source I_1 and current source I_2 are identical and each comprise a constant current value I. The current source I_1 determines a discharge current from the capacitor C_1. The current source I_2 determines a discharge current from the capacitor C_2. A current source I_3 and a current source I_4 are each voltage controlled current sources each comprising a current value that is proportional to the respective common mode voltage of the capacitor C_1 and the capacitor C_2 (i.e., $(V_{C1}+V_{C2})/2$, V_{C1} is the voltage across the capacitor C_1 and V_{C2} is the voltage across the capacitor C_2). A N type field effect transistor (NFET) T_1 and a N type FET T_2 (NFET)are identical FETs. The FET T_1 is turned on and off by the positive pulse INC signal. The FET T_2 is turned

on and off by the positive pulse signal DEC signal. The FET T_1 comprises a parasitic capacitance C_{gd1} between the gate G and the drain D. The parasitic capacitance C_{gd1} between the gate G and the drain D of the FET T_1 is represented by a capacitor 7. The FET T_2 comprises a parasitic capacitance C_{gd2} between the gate G and the drain D. The parasitic capacitance C_{gd2} between the gate G and the drain D of the FET T_2 is represented by the capacitor 9. The voltage control oscillator (VCO) 4 comprises a frequency that is proportional to a difference of the voltages across C1 and C2 (i.e., $V_D = V_{C2} - V_{C1}$, V_D is the voltage difference of the voltages across C1 and C2). Fref is an external reference frequency. A phase of the VCO circuit 4 output (i.e., the frequency) is constantly trying to approach a phase of the external reference frequency Fref. The phase comparator 6 generates the positive pulse signals INC and DEC and determines pulse widths according to a phase difference between the VCO circuit 4 output and the external reference frequency Fref. When a phase of the VCO circuit 4 output is behind a phase of the external reference frequency Fref, a pulse width W_{INC} of the positive pulse signal INC is set wider than a pulse width W_{DEC} of the positive pulse signal DEC. When a phase of the VCO

circuit 4 output is ahead of a phase of the external reference frequency Fref, the pulse width W_{DEC} of the positive pulse signal DEC is set wider than the pulse width W_{INC} of the positive pulse signal INC. For each pair of pulses of the positive pulse signals INC and DEC, the differential voltage (V_D) between C_1 and C_2 is increased by the following quantity: $I*(W_{INC}-_{DEC})/C$. The VCO circuit 4 changes an output frequency according to V_D. A discharge current from C_1 and C_2 must be equal to the constant current value I. Any extra unwanted current (i.e., spark current in description of FIG. 2 as described infra) that is added to the discharge current may cause the phase error to increase; therefore the phase lock loop circuit 1 may become unstable.

[0021] FIG. 2 illustrates the schematic of the sub-circuit 10 for accepting the positive pulse increase (INC) signal of the phase lock loop circuit 1 of figure 1, in accordance with embodiments of the present invention. The following description of sub-circuit 10 also applies to the sub-circuit 11 of FIG. 1. The sub-circuit 10 is a discharge circuit in the charge pump circuit 15 of FIG. 1. The sub-circuit 10 comprises the FET T_1 electrically coupled to both the current source I_1, and the capacitor C_1 as described in the

description of FIG. 1, supra. The positive pulse signal INC is applied to the gate G of the FET T_1. The sub-circuit 10 comprises a basic operation such that when the positive pulse signal INC comprises a logic high, the FET T_1 is turned on and the current source I_1 discharges the capacitor C_1 through the FET T_1. The discharging is terminated when the positive pulse signal INC comprises a logic low thereby turning off the FET T_1. An average discharge current from the capacitor C_1 is dependent upon the current value I, a pulse width W_{INC} of the positive pulse signal INC, and a period of the positive pulse signal INC (i.e., the discharge current from C_1 = the constant current value I multiplied by an amount of time that it takes for the FET T_1 to turn on when the positive pulse signal INC goes from logical low to logical high). The average discharge current from the capacitor C_1 is independent of the voltage across the capacitor C_1 (V_{C1}). In high speed applications for the phase lock loop (PLL) circuit 1, a rise time and a fall time occurring during the transition between logical high and logical low of the positive pulse signal INC are very short. During the rise time and a fall time, the positive pulse signal INC may comprise an extra charge current at the rising edge and an extra discharge current at the falling edge

that may be dissipated through the parasitic capacitance C_{gd1} represented by the capacitor 7 and located between the gate G and the drain D of the FET T_1. The extra charge current or discharge current is called a spark current. The spark current comprises a very high frequency (e.g., about 10 times higher than a frequency of the discharge current from the capacitor C_1). Any spark currents that occur during the rise time and the fall time are not symmetric due to an impedance difference of the FET T_1 during the rise time and the fall time. An average spark current value over a period of the positive pulse signal INC does not equal zero and therefore the average spark current value becomes a part of the average discharge current of the capacitor C_1 making it difficult to control a discharge of the capacitor C_1. A value of the spark current depends upon the capacitance C_{gd1}. The capacitance C_{gd1} depends upon the operation mode of the FET T_1. The operation mode of the FET T_1 is dependent upon on a voltage applied to the drain D (i.e., the voltage across C_1 (V_{C1})) and the voltage applied to the gate G. Therefore the spark current depends on V_{C1}. The spark current is not determined by the current source I_1 and therefore the spark current cannot be controlled. Therefore the PLL circuit 1 may malfunction

because the spark current may dominate the average discharge current of the capacitor C_1. A solution to an elimination of spark current is described in the description of FIG. 3, infra.

[0022] FIG. 3 illustrates a modified schematic for the sub-circuit 10 of FIG. 2 for accepting the positive pulse increase (INC) signal of the phase lock loop circuit 1 of FIG. 1 and eliminating spark current, in accordance with embodiments of the present invention. The following description of the modified schematic for the sub-circuit 10 also applies to the sub-circuit 11 of FIG. 1. A FET T_3 adapted to operate such that the FET T_3 comprises a first impedance value between the source S and the drain D is added to the sub-circuit 10 so that the spark current is passed to ground. Likewise, an additional FET adapted to operate in a similar manner as the FET T_3 is added to the sub-circuit 11 so that spark current is passed to ground. The FET T_3 is an n-channel FET (NFET). The FET T_3 is inserted between T_1 and C_1. A DC voltage VNO is applied to the gate of T_3. The DC voltage VNO is selected from a range of voltages that are less than or equal to minimum voltage across the capacitor C_1 (V_{C1min}) minus a threshold voltage (V_t) of the FET T_3 (i.e., VNO = $V_{C1min} - V_t$) so that the FET operates in

saturation mode (i.e., an operating condition of a FET wherein an increase in the source–drain voltage produces no further increase in drain current) and therefore the FET T_3 comprises the first impedance value between the source S and the drain D. A size of the FET T_3 should be large enough such that a saturation current of the FET T_3 is greater than the current value I (see FIG. 1) of I_1. In high speed applications for the phase lock loop (PLL) circuit 1 of FIG. 1, the rise and fall time occurring during the transition between logical high and logical low of the positive pulse signal INC is shorter than the pulse width of the positive pulse signal INC, so the frequency of the spark current is at least ten times higher than a frequency of the discharge current from the current source I_1. At the node point 28 between the drain D of the FET T_1 and the source S of the FET T_3, a parasitic capacitance C_p represented by the parasitic capacitor 17 and the FET T_3 operating in saturation mode comprising the first impedance value between the source S and the drain D together form a low pass current filter. The parasitic capacitance C_p presents a path comprising a second impedance value for the spark current (i.e., path for the high frequency spark current) so the spark current is passed to ground through the para-

sitic capacitor 17. The first impedance value is at least ten times higher than the second impedance value. The first impedance value may be greater than or equal to one megohm. The second impedance value may be less than or equal to one hundred thousand ohms. The low frequency discharge current from the current source I_1 goes through the FET T_3, the FET T_1, and back to the current source I_1. Therefore the spark current does not combine with the discharge current of C_1.

[0023] While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.